IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	: 10/510,567	Confirmation No.	: 9020
First Named Inventor	: Hirohisa MIYAZAWA		
Filed	: October 8, 2004		
TC/A.U.	: 2841		
Examiner	: TUAN T. DINH		
Docket No.	: 029267.55488US		
Customer No.	: 23911		
Title	: Circuit Board Device for Information Apparatus, Multilayered Module Board and Navigation System		

APPEAL BRIEF

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

On February 19, 2008, Appellant appealed to the Board of Patent Appeals from the final rejection of claims 1, 3 and 5-10. The following is Appellant's Appeal Brief submitted pursuant to 37 C.F.R. § 1.192.

I. REAL PARTY IN INTEREST

An assignment of the present application to Xanavi Informatics Corporation was recorded on October 8, 2004 at Reel/Frame 016355/0871, which represents the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any appeals, interferences or other proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 3 and 5-10 remain pending and are the subject of this appeal. Claims 2, 4 and 11-14 have been cancelled and are not subject to this appeal.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the issuance of the final Office Action on October 18, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

OVERVIEW OF INVENTION

Exemplary embodiments of the disclosed invention are directed to a circuit board structure that can be used in applications such as vehicle information system with navigation functionality. As discussed on pages 2, lines 8-19 of the present application, navigation specifications vary between different vehicle models, and the navigation circuit board must be designed and manufactured in conformance with the different specifications. This requires a great amount of time in the design stage, which results in high production costs.

Exemplary embodiments of the present invention overcome the above-identified and other deficiencies of conventional circuit board structures by providing a circuit board device that includes a base board and one of three types of multilayer module boards that can be mounted on the base board. These

multilayer module boards can be one of a low-end module board, a high-speed module board and an advance function module board. This arrangement allows navigation systems with various functions to be manufactured easily, and reduces production costs. Specifically, this arrangement eliminates the need to design and manufacture a circuit board for each set of specifications from scratch, which reduces costs by reducing the length of time spent in the development stage.

CLAIM 1

Claim 1 is directed to a circuit board device 100 for an information apparatus.[1] The circuit board device 100 includes a base board 200 having mounted thereupon a plurality of low-frequency electronic components.[2] The device also includes a multilayer module board 300 mounted at one surface of the base board and having mounted thereupon a plurality of high-frequency electronic components including at least a CPU 301 and a memory 303.[3] The multilayer module board 300 is one of (i) a low-end module board, (ii) a high-speed module board that operates at higher speed than the low-end module board or (iii) an advanced function module board having more functions than the low-end module board.[4] The base board 200 is connected with one of (i) the low-

[1] Figures 2-4.
[2] Page 10, lines 4-6 and lines 20-23.
[3] Page 10, lines 4-9 and page 11, lines 5-9.
[4] Page 16, lines 10-20.

end module board, (ii) the high-speed module board or (iii) the advanced function module board.

CLAIM 7

Claim 7 depends from 1 due to its dependency from claims 5 and 6. Claim 7 further recites that the four connector terminals 310a-310d each include a narrow, elongated base portion constituted of resin and a plurality of pins 312 fixed to the base portion 311.[5] The four connector terminals are each carried with the base portion 311 attached to a transfer adapter 400 and the four connector terminals 310a-310d are connected through soldering onto a rear surface of the board while attached to the transfer adapter 400.[6]

CLAIM 8

Claim 8 depends from 1 due to its dependency from claims 5 and 6. Claim 8 further recites that the four connector terminals 310a-310d each include a narrow, elongated base portion constituted of resin, a plurality of pins 312 fixed to the base portion, aligning pins 313 projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board, and inclined surfaces 314 for position control formed at both ends of the base portion 311 to be used when soldering the connector terminal.[7] A pair of

[5] Figures 10 and 11, and page 13, lines 10-15.
[6] Figure 9 and page 13, lines 10-25.
[7] Page 13, lines 8-25.

positioning holes 306 at which the aligning pins 313 are loosely fitted are formed at each of four corners of the board.[8] Positions of the connector terminals 310a-310d are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals 310a-310d come into contact with each other while the aligning pins 313 are loosely fitted at the positioning holes 306.[9]

CLAIM 9

Claim 9 is directed to a multilayer module board 300.[10] The board 300 includes a plurality of high-frequency electronic components including a CPU 301 and a memory 303 mounted at, at least, a surface thereof.[11] The plurality of high-frequency electronic components are connected with one another through a wiring pattern formed at an inner layer thereof.[12] An overall shape of the multilayer module board is rectangular and the multilayer module board 300 comprises connector terminals 310a-310d provided as separate members each soldered onto one of four peripheral edges thereof.[13] The four connector terminals 310a-310d each include a narrow, elongated base portion 311 constituted of resin and a plurality of pins fixed to the base portion 311.[14] After the four connector terminals 310a-310d are each carried with the base portion

[8] Page 14, lines 14-17.
[9] Page 15, lines 6-21.
[10] Figures 2-4.
[11] Page 10, lines 4-9 and page 11, lines 5-9.
[12] Page 11, lines 13-15.
[13] Page 13, lines 10-15.

311 attached to a transfer adapter 400, the four connector terminals 310a-310d are connected through soldering onto a rear surface of the board while attached to the transfer adapter 400.[15]

CLAIM 10

Claim 10 is directed to a multilayer module board 300. The board 300 includes a plurality of high-frequency electronic components including a CPU 301 and a memory 303 mounted at, at least, one surface thereof.[16] The plurality of high-frequency electronic components are connected with one another through a wiring pattern formed at an inner layer thereof.[17] An overall shape of the multilayer module board 300 is rectangular and the multilayer module board 300 comprises connector terminals 310a-310d provided as separate members each soldered onto one of four peripheral edges thereof. The four connector terminals 310a-310d each include a narrow, elongated base portion constituted of resin, a plurality of pins fixed to the base portion 311, aligning pins 313 projecting at both ends of the base portion 311 to be used when soldering the connector terminal onto a rear surface of the board, and inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal.[18] A pair of positioning holes 306 at which the aligning pins 313 are loosely fitted are formed at each of four corners of the board.[19] Positions

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[14] *Id.*
[15] Figure 9 and page 13, lines 10-25.
[16] Page 10, lines 4-6 and lines 20-23.
[17] Page 11, lines 13-15.
[18] Page 13, lines 8-25.
[19] Page 14, lines 14-17.

of the connector terminals 310a-310d are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals 310a-310d come into contact with each other while the positioning pins 313 are loosely fitted at the positioning holes 306.[20]

VI. GROUNDS OF REJECTION TO BE REVIEW ON APPEAL

The following grounds of rejection are to be reviewed on this appeal:

1. The rejection of claims 1 and 5 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,477,593 to Khosrowpour et al. ("Khosrowpour");

2. The rejection of claim 3 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Khosrowpour and U.S. Patent No. 6,085,137 to Aruga et al. ("Aruga"); and

3. The rejection of claims 6-10 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Khosrowpour and U.S. Patent No. 5,346,402 to Yasuho et al. ("Yasuho").

[20] Page 15, lines 6-21.

VII. ARGUMENT

As will be described in more detail below, the anticipation rejection of Appellant's claims is based on a misapplication of the relevant law, and the obviousness rejections are improper for failure to present any evidence to support the conclusion of obviousness. These issues have addressed in Appellant's replies to the Office Actions and the Request for Pre-Appeal Brief Conference and these arguments are herein incorporated by reference.

A. The Rejection of Claims 1 and 5 for Anticipation by Khosrowpour is Improper

The anticipation rejection of claims 1 and 5 in view of Khosrowpour is improper because Khosrowpour does not expressly or inherently disclose all of the elements of these claims. Specifically, Khosrowpour does not expressly or inherently disclose a circuit board device for an information apparatus comprising:

1. a multilayer module board;
2. a multilayer module board including at least a CPU and a memory; and
3. the multilayer module board that is one of (i) a low-end module board, (ii) a high-speed module board that operates at higher speed than the low-end module board or (iii) an advanced function module board having more functions than the low-end module board.

1. The Law of Anticipation

It is well established that anticipation requires a single prior art reference that expressly or inherently discloses each and every claim elements.[21] Specifically, the "identical invention must be shown in as complete detail as is contained in the ... claim."[22]

Inherency is not established by probabilities or possibilities, but instead requires that the extrinsic evidence makes "clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."[23] Accordingly, the "mere fact that a certain thing may result from a given set of circumstances is not sufficient."[24]

2. <u>The Disclosure of Khosrowpour</u>

Khosrowpour discloses a stacked input/output bridge circuit assembly having flexibly configurable connections. Specifically, daughterboards 120 and 130 can be stacked on motherboard 110. (Col. 4, lines 12-13). The daughterboards "may comprise boards employing using through-hole or surface-mounted devices on single or multi-layer printed circuit boards (PCBs), as well as more exotic board structures constructed using, for example, thick-film or co-fired ceramic technologies." (Col. 4, lines 17-21). Khosrowpour does not,

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[21] See, for example, M.P.E.P. § 2131 and *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[22] M.P.E.P. § 2131 quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[23] M.P.E.P. § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).
[24] *Id.*

however, disclose that daughterboards 120 and 130 include at least a CPU and memory, or that they are one of a low-end module board, a high-speed module board or an advanced function module board.

3. Khosrowpour Does Not Expressly or Inherently Disclose a Multilayer Module Board

The Patent Office relies upon daughterboard 120 of Khosrowpour as corresponding to the claimed multilayer module board, but acknowledges that Khosrowpour does not *explicitly* disclose that daughterboard 120 is a multilayer board. Instead, the Patent Office asserts that daughterboard 120 is inherently a multilayer board. To support this position the Patent Office cites U.S. Patent No. 5,025,306 to Johnson et al ("Johnson") as extrinsic evidence that the daughterboard of Khosrowpour is inherently a multilayer board.

Thus, Johnson must make "clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."[25] In other words, Johnson must make clear that *all daughterboards* are multilayer boards. If, on the other hand, Johnson only discloses that *one type* of daughterboard is a multilayer board, then the Patent Office's position is based "mere fact that a certain thing may result from a given set of circumstances [which] is not sufficient."[26]

[25] M.P.E.P. § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).
[26] *Id.*

Johnson discloses an assembly of semiconductor chips that includes daughterboard 88, which "includes multilayers of conductors and insulator material."[27] Thus, Johnson does disclose *one type* of a daughterboard that is a multilayer board. Johnson does not, however, disclose that *all daughterboards must* be multilayer boards. Without such a disclosure, Johnson does not make "clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."[28]

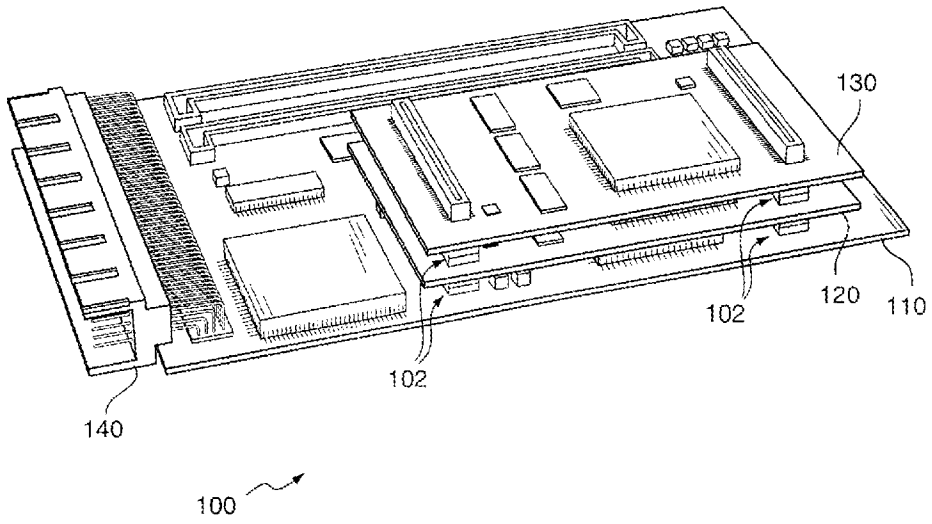
This argument was presented in Appellant's Reply filed on January 17, 2008. Instead of providing a response to this argument, the Advisory Action merely states that the previous grounds of rejection are maintained. Accordingly, the Patent Office has presented no evidence to support its inherency position, and for the reasons set forth above this position is not supported by the evidence of record.

[27] Column 4, lines 2-4.
[28] M.P.E.P. § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

4. **Khosrowpour Does Not Expressly or Inherently Disclose a Multilayer Module Board Including at Least a CPU and a Memory**

The rejection of claim 1 relies upon Figure 1 of Khosrowpour (reproduced below) for the disclosure of daughterboard 130 including at least a CPU and a memory.

FIG. 1



Specifically, the Response to Arguments section of the final Office Action asserts that the unlabeled "bigger chip" discloses the claimed CPU and the unlabeled "three chip reside near to the square chip" corresponds to the claimed memory.

In addition to not including a label for the "bigger chip" or the "three chip reside near to the square chip" in Figure 1, Khosrowpour does not describe these components in the specification. Thus, there is no express disclosure in

Khosrowpour that daughterboard 130 includes a CPU and memory, or as the Patent Office asserts, that the unlabeled "bigger chip" is a CPU and the unlabeled "three chip reside near to the square chip" is a memory.

In view of the lack of express disclosure of daughterboard 130 including a CPU and memory, Appellant's claim 1 can only be anticipated if this is inherent from the disclosure of Khosrowpour. The Patent Office has provided no reasoning or extrinsic evidence to support the position that in Figure 1 of Khosrowpour the unlabeled "bigger chip" *must be* a CPU and the unlabeled "three chip reside near to the square chip" *must be* a memory. Accordingly, the Patent Office has not met its burden in establishing that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."[29] As such, the Patent Office has not provided sufficient evidence establishing that the unlabeled "bigger chip" *must be* a CPU and the unlabeled "three chip reside near to the square chip" *must be* a memory. Instead, it appears that the Patent Office must be relying upon the possibility that the unlabeled "bigger chip" *could be* a CPU and the unlabeled "three chip reside near to the square chip" *could be* a memory. Inherency, however, is not established merely because "a certain thing may result from a given set of circumstances."[30]

[29] M.P.E.P. § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).
[30] *Id.*

5. Khosrowpour Does Not Expressly or Inherently Disclose the Type of Claimed Multilayer Module Board

Appellant's claim 1 recites that the multilayer module board mounted on a base board, and is one of a low-end module board, a high-speed module board or an advanced function module board.

Again, the rejection of claim 1 relies upon daughterboard 120 of Khosrowpour as disclosing the claimed multilayer board. Apart from describing the bus interface circuits and the composition of the boards themselves, Khosrowpour does not describe the type of function performed by daughterboard 120. Accordingly, Khosrowpour does not disclose that daughterboard 120 is one of a low-end module board, a high-speed module board or an advanced function module board. Nor does Khosrowpour disclose that motherboard 110 can accept more than one different type of board. In contrast, the base board of Appellant's claim 1 can accept a number of different types of multilayer module boards. The Patent Office has provided no explanation or extrinsic evidence to support the position that Khosrowpour includes an express or inherent disclosure of the type of boards recited in Appellant's claim 1.

B. The Rejection of Claim 3 for Obviousness in View of the Combination of Khosrowpour and Aruga is Improper

Claim 3 depends from claim 1. As discussed above, Khosrowpour does not disclose all of the elements of Appellant's claim 1. It is respectfully submitted that Aruga does not remedy the above-identified deficiencies of Khosrowpour with respect to claim 1. Accordingly, even if one skilled in the art were motivated to combine Khosrowpour and Aruga, the combination would not render claim 1, and in turn dependent claim 3, obvious.

C. The Rejection of Claims 6-10 for Obviousness in View of the Combination of Khosrowpour and Yasuho is Improper

Claims 6-8 variously depend from claim 1. As discussed above, Khosrowpour does not disclose all of the elements of Appellant's claim 1. It is respectfully submitted that Yasuho does not remedy the above-identified deficiencies of Khosrowpour. Accordingly, the combination of Khosrowpour and Yasuho cannot render claims 6-8, which depend from claim 1, obvious.

Regarding claims 7-10, for the following additional reasons it is respectfully submitted that the combination of Khosrowpour and Yasuho does not disclose or suggest all of the elements of these claims.

Dependent claim 7 and independent claim 9 both recite four connector terminals that "are each carried with the base portion attached to a transfer adapter and the four connector terminals are connected through soldering onto a

rear surface of the board while attached to the transfer adapter." The Office Action relies upon Yasuho as disclosing this claim element. The Office Action, however, does not indicate where a disclosure of the claimed four connector terminals can be found in Yasuho. Appellant's Reply filed on January 17, 2008, requested that the Patent Office provide a citation to Yasuho for the disclosure or suggestion of the claimed four connector terminals. Instead of providing such a citation, the Advisory Action merely states that the "Examiner maintains the final Office action mailed on 10/18/07." Thus, the Patent Office has not yet provided any evidence that Yasuho discloses or suggests the claimed four connector terminals. Without any such evidence, the Patent Office has not yet established a *prima facie* case of obviousness. Because Khosrowpour and Yasuho both do not disclose or suggest the claimed four connector terminals, the combination does not render claims 7 and 9 obvious.

Dependent claim 8 and independent claim 10 both recite

> the four connector terminals each include
>
> ***
>
> aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and
>
> ***
>
> a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and

The Office Action relies upon Yasuho as disclosing the four connector terminals including aligning pins and the pair of positioning holes. The Office Action, however, does not indicate where a disclosure of the claimed four connector terminals and pair of positioning holes can be found in Yasuho. Again, Appellant's Reply filed on January 17, 2008 requested that the Patent Office provide a citation to Yasuho for the disclosure or suggestion of the above-identified elements of claims 8 and 10, and the Advisory Action ignored this request.

Because Khosrowpour and Yasuho both do not disclose or suggest the claimed four connector terminals or pair of positioning holes, the combination does not render claims 8 and 10 obvious.

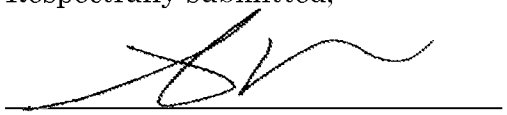
VIII. CONCLUSION

Because the patent relied upon for the anticipation rejections fails to include an express or inherent disclosure of every element of claims 1 and 5, this rejection should be reversed. Likewise, because the obviousness rejections of claims 3 and 6-10 do not include a prior art disclosure of every claim element, these rejections should be reversed.

The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, to Deposit Account No. 05/1323, Docket No.: 029267.55488US.

Respectfully submitted,

May 14, 2008



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CLAIMS APPENDIX

1. A circuit board device for an information apparatus comprising:

a base board having mounted thereupon a plurality of low-frequency electronic components; and

a multilayer module board mounted at one surface of the base board and having mounted thereupon a plurality of high-frequency electronic components including at least a CPU and a memory, wherein:

the multilayer module board is one of (i) a low-end module board, (ii) a high-speed module board that operates at higher speed than the low-end module board or (iii) an advanced function module board having more functions than the low-end module board; and

the base board is connected with one of (i) the low-end module board, (ii) the high-speed module board or (iii) the advanced function module board.

2. (Cancelled)

3. A navigation system comprising a circuit board device for an information apparatus according to claim 1.

4. (Cancelled)

5. The multilayer module board used in the circuit board device for an information apparatus according to claim 1, comprising:

a plurality of high-frequency electronic components including a CPU and a memory mounted at, at least, a surface thereof, wherein:

the plurality of high-frequency electronic components are connected with one another through a wiring patterns formed at an inner layer thereof.

6. The multilayer module board according to claim 5, wherein an overall shape of the multilayer module board is rectangular and the multilayer module board comprises connector terminals provided as separate members each soldered onto one of four peripheral edges thereof.

7. The multilayer module board according to claim 6, wherein:

the four connector terminals each include a narrow, elongated base portion constituted of resin and a plurality of pins fixed to the base portion; and

the four connector terminals are each carried with the base portion attached to a transfer adapter and the four connector terminals are connected through soldering onto a rear surface of the board while attached to the transfer adapter.

8. The multilayer module board according to claim 6, wherein:

the four connector terminals each include

a narrow, elongated base portion constituted of resin;

a plurality of pins fixed to the base portion;

aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and

inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal;

a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and

positions of the connector terminals are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the aligning pins are loosely fitted at the positioning holes.

9. A multilayer module board comprising:

a plurality of high-frequency electronic components including a CPU and a memory mounted at, at least, a surface thereof, wherein:

the plurality of high-frequency electronic components are connected with one another through a wiring pattern formed at an inner layer thereof;

an overall shape of the multilayer module board is rectangular and the multilayer module board comprises connector terminals provided as separate members each soldered onto one of four peripheral edges thereof;

the four connector terminals each include a narrow, elongated base portion constituted of resin and a plurality of pins fixed to the base portion; and

after the four connector terminals are each carried with the base portion attached to a transfer adapter, the four connector terminals are connected through soldering onto a rear surface of the board while attached to the transfer adapter.

10. A multilayer module board comprising:

a plurality of high-frequency electronic components including a CPU and a memory mounted at, at least, one surface thereof, wherein:

the plurality of high-frequency electronic components are connected with one another through a wiring pattern formed at an inner layer thereof;

an overall shape of the multilayer module board is rectangular and the multilayer module board comprises connector terminals provided as separate members each soldered onto one of four peripheral edges thereof;

the four connector terminals each include

a narrow, elongated base portion constituted of resin;

a plurality of pins fixed to the base portion;

aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and

inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal;

a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and

positions of the connector terminals are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

Claims 11.-14. (Canceled)

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None